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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	White	Docket No:	TI-31770
Serial No:	09/817,695	Examiner:	Smith, Tyrone W.
Filed:	03/26/01	Art Unit:	2837
For:	DISK DRIVE SERVO ARM RETRACT AND SPINDLE BRAKE CIRCUIT		

APPEAL BRIEF PURSUAINT TO 1.192(c)

Assistant Commissioner For Patents
Washington, DC 20231

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at **703-308-3431** on 5-21-03 :

Tommie Chambers

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JS

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Final Rejection mailed November 27, 2002, and the Advisory Action mailed February 28, 2003.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellant's legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-5 were originally filed, and no claims have been canceled. Thus, the subject matter of the instant appeal is the final rejection of Claims 1-5.

STATUS OF AMENDMENTS

Again, the application was originally filed with Claims 1-5. By virtue of an amendment filed on March 19, 2002, Claims 1-3 and 5 were amended. An amendment after final was filed on February 17, 2003, amending no claims.

The advisory action indicated that the response was considered.

SUMMARY OF THE INVENTION

The present invention uses a three zone operation for a power fault or other emergency condition. During the first zone of operation, the head motion is stopped. This prepares the head for retract especially if the head is moving away from the retract area. The operation during zone two is to bring the head back to the landing area. Lastly, the operation during zone 3 is to slow down and stop the spindle motor.

Turning now to Figure 1, a voice coil motor (VCM) control circuit 100 includes switches 104 and switch 106 are switch circuits which operate in accordance with a particular state during the retract period. Switch 104 connects the op amp 102 to the NFET 108 during the pulse state or during the high state. During the low state the gate of NFET 108 is connected to ground through switch 104. Likewise, switch 106 during the pulse state or the high period connects ground to the gate of NFET 110. During the low state the gate of NFET 110 is connected to voltage V_{10}. The gate of NFET 114 is connected to ground, and the gate of NFET 112 is connected to voltage V_{10}. The drain of NFET 108 and the drain of NFET 114 are connected to Voltage V_{ISO}. The source of NFET 108 is connected to the VCM motor at terminal V_{CMN}. The source of NFET 114 is

connected to terminal V_{CMP} at the other end of the VCM motor. The drain of transistor 110 is connected to terminal V_{CMN} and the drain of NFET 112 is connected to the terminal V_{CMP}. The source of NFET 110 and the source of NFET 112 are connected to ground. An operational amplifier 102 has a plus input to receive a set signal $2XV_{RET}$. The negative input to op amp 102 is connected to the source of NFET 108 and terminal V_{CMN}. The output of op amp 102 is connected to switch 104, which during either the pulse or high state connects the output of op amp 102 with the gate of NFET 108. During the low state, the gate of NFET 108 is connected to ground through switch 104. The op amp 102 compares the signal $2XV_{REC}$ with the voltage V_{CMN}. Thus, during the pulse or high state terminal V_{CMN} is held at signal $2XV_{RET}$. NFET 112 has a voltage V_{10} applied to the gate, which keeps NFET 112 shorted between drain to source, which keeps the terminal V_{CMP} at ground. The NFET 114 remains open from drain to source because the gate of NFET 114 is connected to ground. Thus, during the low state, the NFET 110 shorts V_{CMN} to ground from source to drain.

Figure 2 illustrates the spindle motor control circuit 200 during the retract period. Switch 202 operates in accordance with the particular state during the retract period. During the pulse state or the high state the op amp 204 is connected to the gate of NFET 212, the gate of NFET 214 and to the gate of NFET 216. During the low state the gate of NFET 212, NFET 214 and the gate of NFET 216 is connected to voltage V_{10} which shorts the terminal 222 terminal 220 and terminal 218 to ground. The terminal 218 and the terminal 220 and the terminal 222 as show in Figure 7 connect the phases of the motor 700 shown connected in Δ. NFET 212, NFET 214 and NFET 216 are considered the low end switches while NFET 230, NFET 232 and NFET 234 are considered the high side switches for the spindle motor 700. Figure 2 illustrates the gates of NFET 230, NFET 232 and NFET 234 connected to ground to keep these NFETs from conducting during the emergency operation. Terminal 222 is connected between the source of NFET 230 and the drain of NFET 212. Likewise terminal 220 is connected between the source of NFET 232 and the drain of NFET 214. The drain of transistor 230 is connected to the drain of transistor 232 and is connected to the drain of transistor 234. The drain of transistor NFET 230, the drain of NFET 232 and the drain of NFET 234 are connected to

voltage V_{ISO}. Additionally, a parasitic diode 240 is connected between the drain and source of transistor 230. Diode 242, which is parasitic, is connected between the drain and source of transistor 232 and a parasitic diode 244 is connected between the drain and source of transistor 234. A capacitor 235 is connected to drains of transistors 230, 232 and 234. This capacitor maintains volts. The source of NFET 212, the source of NFET 214 and the source of NFET 216 is connected to ground. Terminal 222 connected to resistor 211 through diode 250, the terminal 220 is connected to resistor 211 through diode 252, and the terminal PHW 218 is connected to resistor 211 through diode 254. Additionally, the center point of a voltage dividing circuit 209 is connected to the negative input of operational amplifier 204. The voltage dividing circuit 209 includes resistor 208 connected to ground and connected to the center point of the voltage dividing circuit 209 and resistor 210 connected to the center point of voltage dividing circuit 209 and to switch 206. While in the low state, the gates of NFET 212, NFET 214 and NFET 216 are connected to voltage V_{10}. As the motor turns, voltages are generated within the coils and these voltages result in currents flowing to ground as a result of the shorted NFETs on the low end namely, NFET 212, NFET 214 and NFET 216. During the transition from the low state to the pulse state, switch 202 switches to connect the output of operational amplifier 204 to the gate of NFET 212, NFET 214 and NFET 216. Likewise, the switch 206 switches to the terminal to input voltage V_{10}. A reduced V_{10} is input to the negative terminal of op amp 204. The reduced V_{10} is a result of the voltage dividing circuit 209. The plus terminal of op amp 204 is essentially at ground. The op amp 204 outputs a voltage, which immediately opens NFET 212, NFET 214 and NFET 216 drain to source. Again since these NFETs are connected to large inductors, namely the windings of the spindle motor as illustrated in Figure 7, these currents produce a large voltage which is known as a flyback voltage and overcome the threshold voltage of diode 240, the threshold voltage of diode 242 and the threshold voltage of 244. Consequently, the voltage V_{ISO} increases sharply as a result of the flyback voltage. The increased voltage V_{ISO} increases the voltage V_{10}. As the voltage at terminal 222, terminal 220 and terminal 218 approach the reduced voltage V_{10}, the voltage across resistor 211 increases, increasing the output from operational amplifier 204. At the end of the pulse state and the beginning of the high state, switch 206 switches to a new voltage $V2XV_{RET}$. This is

generally a smaller voltage than V_{10}, and consequently the voltage at terminal 222, terminal 220 and terminal 218 is reduced to correspond to the new voltage as a result of the operation of op amp 204 and the feedback of the voltage of terminals 218, 220 and 222. At the end of the high period the switch 202 is switched to the low state and the voltage at gates of NFET 212, NFET 214 and NFET 216 rise to V_{10} so that the switches short between the drain to source. As a consequence, the terminal 222, terminal 220 and terminal 218 are at ground and the motor 700 brakes at ground. thus, the cycle can be repeated if desired. As mentioned above, Figure 4 illustrates a circuit to generate voltage V_{10}. Voltage V_{ISO} is input to diode 404, and the output of diode 404 is input to regulator 402, which generates the voltage V_{10}.

Figure 3 illustrates the relationship between the voltage V_{RET} and voltage $V2XV_{RET}$. The pulses which correspond to signal voltage $V2XV_{REC}$ has a fifty percent (50%) duty cycle and correspondingly has twice the magnitude of voltage V_{RET}.

Turning now to Figure 6, Figure 6 illustrates the SPM phase voltage at each of terminal 222, terminal 220 and terminal 218. Additionally, the voltage V_{ISO} is illustrated. Voltage V_{10} is illustrated as well as the voltage across the VCM motor VCMN and voltage VCMP. As illustrated in Figure 6, the SPM voltage is zero during the low state, rises sharply during the pulse state and is reduced during the high state. The voltage V_{ISO} increases sharply during the pulse state. The voltage V_{10} decreases during the VCM dynamic brake and increases during the pulse state of the retract. Even though the spindle motor can be turning at a relatively low velocity, which occurs near the end of the power down stage, the high voltages as illustrated in Figure 6 by the SPM phase voltage and the voltage V_{ISO} during the pulse period can be achieved. The diodes 240 and 242 and 244 typically are parasitic drain to source diodes and it is necessary to place a capacitor across the VISO node for power supply during power interruption or power reductions. The present invention allows this capacitor 235 to be smaller in size since the pumping can force a larger voltage onto the capacitor in a short amount of time. Furthermore, the lower capacitance reduces the inrush of current through the diode and into the capacitor. During the low state the motor is braked by the shorting of the phasing

to ground. Typically the dynamic brake of the voice coil motor VCM is performed for at least ten milliseconds. This dynamic brake shorts the connections of the servo arm coil, namely terminal V_{CMN} and terminal V_{CMP} together. The pulse state is begun and the voltage V_{ISO} and the generated supply referred to as voltage V_{10} are used for power. The retract period is terminated when the back EMF indicates that the motor has slowed to a desired speed or a counter can be used to provide a specific time for the retract period. Next, the spindle dynamic brake is initiated and the phases of the spindle motor (spm) are shorted together.

ISSUES

The two issues on appeal are first whether Claims 1 and 3-5 are unpatentable under 35 U.S.C. § 103 over Yoshida in view of Choi; and secondly whether Claim 2 is unpatantable under 35 U.S.C. § 103 over Yoshida in view of Choi and Carobolante.

GROUPING OF THE CLAIMS

Claim 1 as contained in the attached appendix is independently patentable, and this claim does not stand or fall together for the reasons more clearly set forth herein below.

ARGUMENTS

It is respectfully submitted that Yoshida does not disclose or suggest the presently claimed invention including the motor breaking during the low voltage state, the control circuit receiving or a flyback voltage from the motor during the pulse voltage state, and the control circuit receiving the reduced flyback voltage from the motor during the high voltage state.

Yoshida does not disclose a flyback voltage and does not disclose the voltages associated with motor breaking. Yoshida discloses voltages for driving a motor such as described in the first seven lines of column 5.

The Examiner alleges that Yoshida controls the motor in three different voltage states, referring to Figure 1 elements 15 and 20.

Notwithstanding the allegations of the Examiner, as indicated at column 6, line 9, et seq, Yoshida discloses power supply 20 having supply voltages 16, 17, and 18. Additionally, Yoshida discloses that supply voltages selectively means 18 selects one of the supply voltages. The supply voltage is supplied to the spindle motor.

The Examiner alleges that deceleration is equivalent to braking the motor.

Applicants traverse.

Deceleration could mean coosting which is not braking.

This does not disclose the above noted claimed subject matter.

Choi does not disclose or suggest the presently claimed invention including the motor breaking during the low voltage state and the control circuit receiving the flyback voltage from the motor during the pulse voltage state, the control circuit receiving a reduced flyback voltage being reduced from the flyback voltage from the motor during the high voltage state.

Choi does not disclose breaking and does not disclose a three voltage state circuit.

The Examiner alleges that Choi discloses changing, reduced or altered.

How does this related to the claimed invention?

It does not. The claimed invention relates to low, high, and pulsed voltage state.

Whether or not Carobolante discloses the limitation of Claim 2 and whether or not one of ordinary skill in the art would consider modifying the teachings of Yoshida or Choi is of no moment since the result in construction would no way disclose or suggest the above mentioned subject matter.

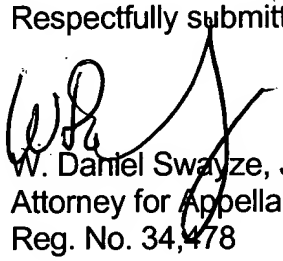
Claims 1-5 patentably define over the applied art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-5 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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